CLOAD
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Once Upon a Time,

There was a computer nut out in Southern California. He liked to play with software, but his real interest was hardware. He started the first machine - readable magazine, named CLOD, or something of the sort, and immediately became involved in paperware. Among other unique attributes, this magazine was always late. At first, this was due to technical reasons involved with the duplication process, compounded with a lack of ability to come up with publishable material fast enough. Then, again for technical reasons this magazine decided to go "in-house" for cassette duplication. This moved the schedule from a steady, reliable one month late to an innovative four months late. As soon as the duplicating equipment was built, his paperware was the only holdup. Then he escaped. He hacked his leg irons in half with a sharp data file, jumped into an airplane, and flew to Wolf Point, Montana to see the recent solar eclipse. Upon return, what is facing him but yet another issue, ready to go except for the paperware. (Sigh). We're catching up, though - I'm told that this is the February issue going out.

More on that eclipse trip - a party of three, including CLOAD's first editor, a mutual friend and myself flew a Cessna Cardinal up to the area where the eclipse would be total. The reason for not flying by commercial airline was that we didn't know where we were going, and wouldn't know until after we got there. (Weather was our prime concern - Northern Montana and Southern Canada are not noted for nice weather in February.) As part of our equipment, we had a level II TRS-80 on board, which was rigged up to run off the airplane's battery. The main purpose for it was to provide us with real - time data on the eclipse, such as time, duration, altitude and azimuth (which are different for different locations). Our plan of last resort was to actually climb up and see the eclipse from the aircraft. The best laid plans, however, gang aft a-gley and all that... the best spot available was a clear spot around Wolf Point, Montana, and even that location had some thin, high clouds that were a lot higher than we could fly. So, we viewed it from the airport at Wolf Point. Those of you who ever get the chance to see a total eclipse should do so. It gives you an excuse to travel and a chance to see a rare and beautiful, though somewhat short sight.

Announcements:

Radio Shack has changed their cassette load circuitry to make loading level II tapes much easier. Basically what the change amounts to is to replace the input amplifier chip (Z4) and a dozen or so resistors and capacitors with a transistor circuit. The new circuitry is available as a retrofit - it can be installed in all the existing TRS-80's. The changes (I've been told) are available through your local Radio Shack dealer. We have been furnished a copy of the modification, and will give a copy of the copy to anyone who sends a stamped, self - addressed envelope to us marked "Cassette Circuit Modification". (We originally planned to publish it, but it's too big.) We will also throw in a copy of our own cassette recorder modification, which modifies the CTR-41 to allow listening to the CLOAD and (thanks to Dave Passwaiter) CSAVE bit stream.

From our editor - apologies for not being as punctual as he would like to be in replying to those people who have sent in submissions. Seems that he has been pressed into service as the duplicator operator, and this leaves him about 40 hours a week for things like food and sleep.

Bug - in October's level I "Graph", delete line 56. Line 55 should read: 55 IF P.(X,Y) T.R.(X,Y) : R.(128-X,Y) : R.(X,48-Y) : R.(128-X,48-Y) : G.10

Hardware:

O.K, folks, here it is. The schematic following this letter is the 8255 interface that I've been promising for awhile. I'd like to talk a bit on what the circuit is and how it works, leading up to the point of how to hook it into something useful.

The drawing (formally speaking, a circuit schematic diagram) is really only a glorified road map for electrons. The lines drawn between the various parts represent wires, through which electricity travels. On any line, at any given time, the voltage is either high or low (explained in last month's CLOAD, as well as in every digital "intro" book). Each part, therefore, can be looked upon as a routing station. Each has one or more input connections (pins) through which it listens to other parts talking. Each also has one or more output pins, through which it talks to the rest of the circuit. As a general sort of rule, two outputs are not normally connected together on one line. They tend to get into arguments. Likewise, though several inputs can all be connected together on one line, it will be a very quiet line if there isn't at least one talker. Not always mentioned, but always there, are the +5V supply and ground pins. These have to be hooked up or the chip has a hard time doing anything. If you can imagine a Howard Johnson's without electrical power, you've got the idea.

Let's look at a few parts. The first part of interest looks like triangle pointing to the right, with a bubble on its nose. This is an inverter. What it does is look at the input line (to the left in this drawing), and force the output line the other way. Low (0) in, high (1) out. High in, low out.

The next part is a "nand" gate. This looks more like a bubble - nosed bullet than a gate to me, but I didn't get to name them. What a "nand" gate does is look at its input lines, and if they are all high, it puts a low on its output line. No democratic voting here. If all inputs are high, it outputs a low. If any of the several input pins are low, it outputs a high.

The last significant part in the circuit is the 8255 itself. It's the large rectangle. If a part is more complex than an inverter or a gate, it is drawn as a box, and must be labeled. Let's check out all the pins on the left side of the 8255. We start at the top (where else ?). The first eight pins are the data pins, and are connected to the data bus. In the TRS-80, the data bus is bidirectional. This means that these pins are allowed to be (and in this case, are) both listeners and talkers, though not both simultaneously. The TRS-80 lets the chip know what to be at any given microsecond. This is the pathway over which all information is sent, both to and from the Z-80 inside the TRS-80. There being eight lines provided, eight bits (one byte) of information can be sent at a time, making the TRS-80 an "eight bit machine".

There are two pins immediately below the address bus. These are the address pins, numbered 8 and 9 for A1 and A0, respectfully. There are four possible combinations of voltage on these pins, (00,01,10,11) and each combination selects one of the four ports available inside the 8255 (A, B, C, and Control, respectfully).

The next pin down is the input control (pin 5, labeled $\overline{RD}$). If this pin is pulled to a low level (it's usually high) the 8255 will go into the input condition, which means it sends information to the TRS-80. Please note the terminology. When we speak of input and output with respect to the flow of information, we always call it from the viewpoint of the Z-80 chip (For present purposes, Z-80, TRS-80, and CPU are synonymous). Thus the 8255 inputs data to the TRS-80, and outputs data from it. This may seem confusing, but it is consistent, and it keeps designers from becoming alchoholics. Well, tends to.

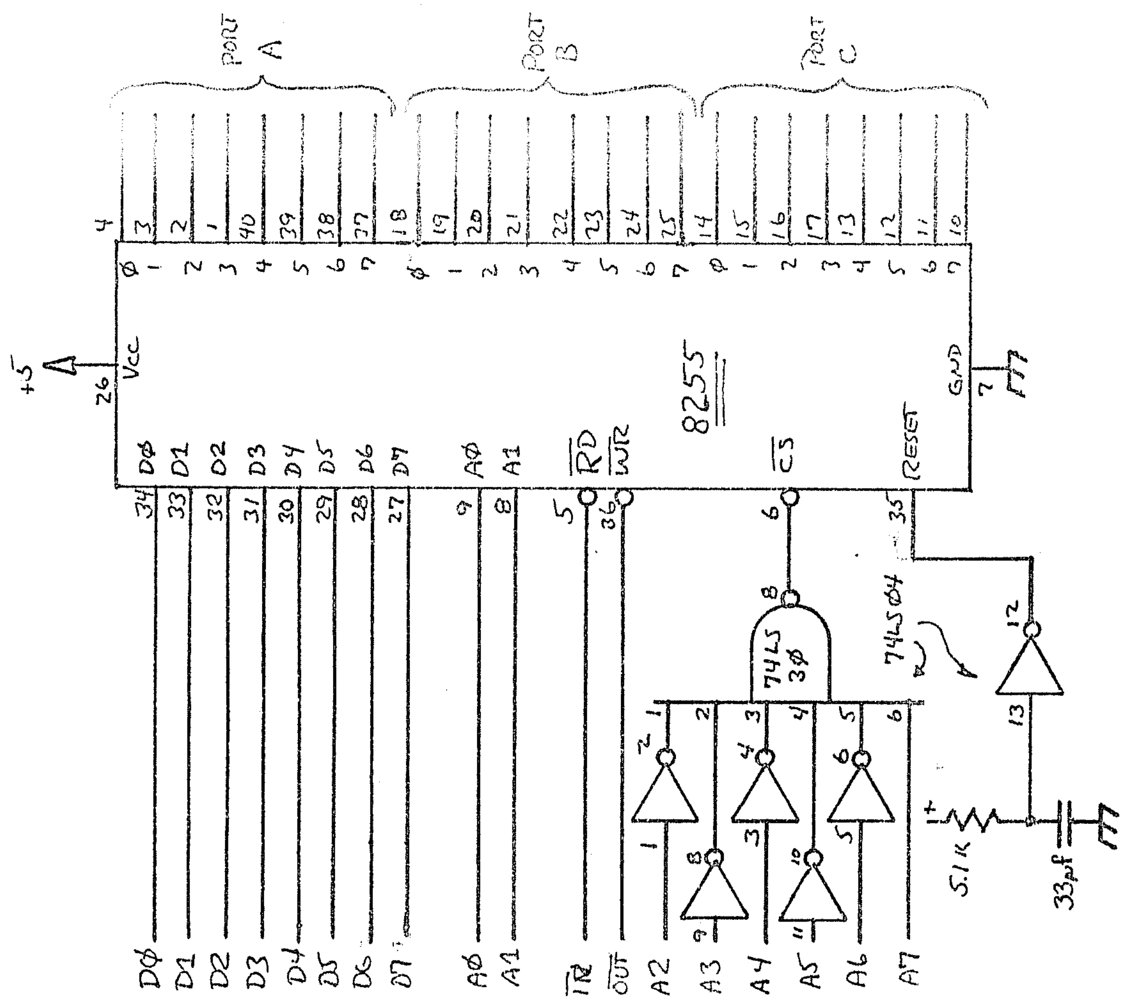
Moving right along, we drop down to the output control pin (pin 36, labeled $\overline{WR}$). This pin is also normally high, and is pulled low to put the 8255 into the output mode. As you might guess, the input control and output control pins are never pulled low at the same time.

Next we see the chip select (pin 6, labeled $\overline{CS}$). This pin must be pulled low to wake up the 8255. If this one isn't low, the other inputs (except RESET) won't do anything at all. Examining the circuitry leading to this pin, we see that it is pulled low when A7 is high, and A6 through A2 are low. This occurs, among other times, when we program OUT 128,X (or 129,130,and/or 131). During the "INP(port number)" and the "OUT port number,value" instructions, lines A0 through A7 have a binary voltage pattern on them which corresponds to the port number.

The last input line is the line we activate when powering up the interface (pin 35, labeled RESET). It is (for a change) normally held low. If this pin is raised to a logical "1" and then pulled low again, the 8255 will clear all its internal registers and switch all its I/O pins (right side) to the input mode. The resistor (squiggly line) and the capacitor (parallel horizontal lines) with an inverter cause this to happen when the power is turned on.

We've got about an inch left, so let's see what the TRS-80's expansion port looks like when we execute an OUT 131,43. The BASIC instruction sets up the Z-80 to output the pattern "43" (00101011 binary) to port number 131 (10000011). The sequence is as follows: The Z-80 chip outputs this 10000011 pattern on the lower address lines (A0 - A7). The most significant six lines cause a low on the $\overline{CS}$ input of the 8255 because of the action of the inverters and the nand gate, which lets the 8255 know that it's time to wake up. The least significant two address lines go directly to the 8255, and select the Control port inside as the destination. Next, the Z-80 puts the pattern 00101011 on the data bus. This is the value - decimal 43 - that is to be transferred. After about a microsecond, the Z-80 pulls the $\overline{OUT}$ line low. The 8255 now swallows the byte. Tune in next issue and we'll discuss what it does with it.

Ralph McElroy
Publisher



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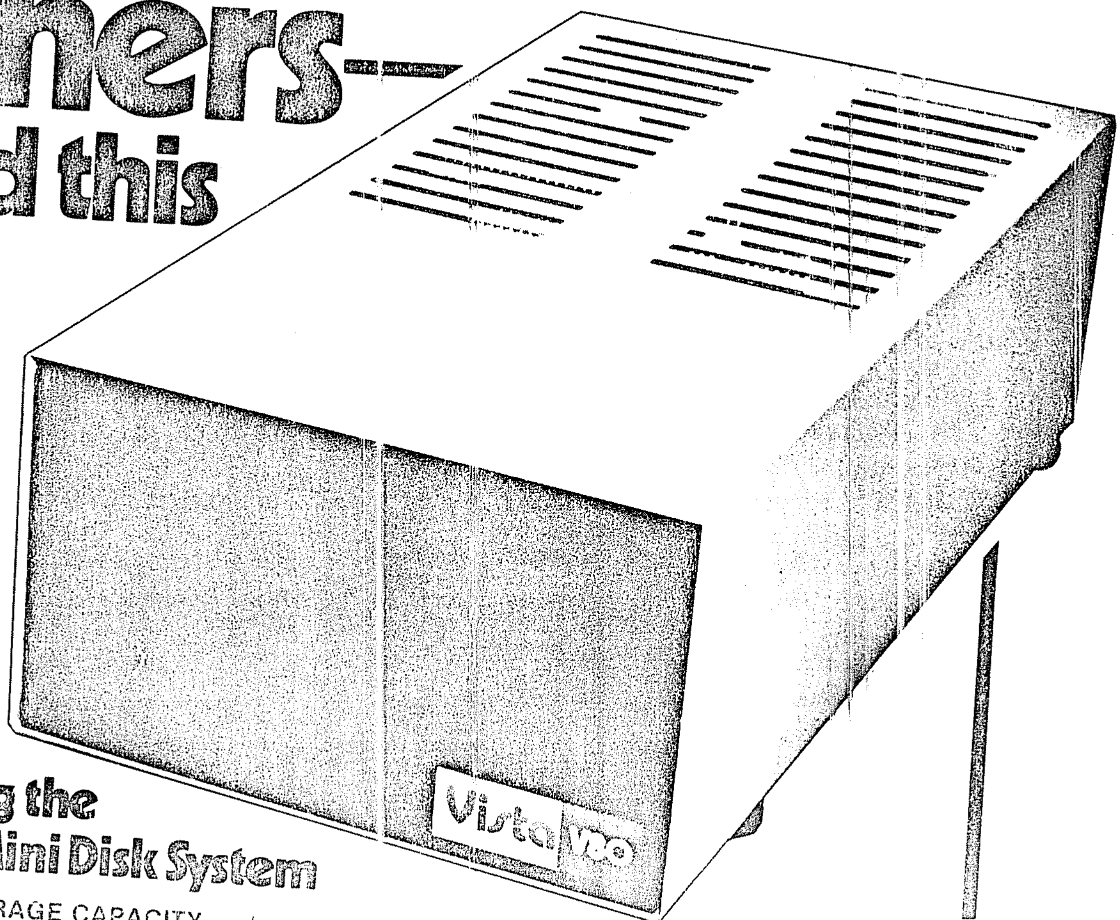

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